

Booth Multiplier Based on Low Power High Speed Full Adder With F_{in_FET} Technology

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Abstract— This paper proposes a novel F_{in} FET-based HSFA for the multiplier in order to overcome the issues of low speed operation. It is advantageous to use F_{in} FETs to construct the arithmetic circuit while assessing the available works. The carry propagation and slow operation of the old technique are disadvantages. The CMOS-based compressor circuit, on the other hand, suffers from leakage current, which reduces its driving capabilities. High current DSP applications are well matched to the design's specifications. Even with a supply voltage of 1 volt, the proposed device has a decent driving capability. As a result, the circuit runs more quickly and has less latency. A transmission gate is used in the design of the suggested adder structure to selectively block or transfer data from the input to output. Half adder and adder are shown in the following illustrations. The smaller the transistor count, the less power it uses. The suggested F_{in} FET design for the smaller transistors has a superior driving capability than the CMOS equivalent. Additionally, when cascading, the F_{in} FET based adder may contribute to superior switch performance, such as when using ripple carry adder. There is also the possibility of a low operation, which may operate at Low wattage Electronic designs for high-performance and small devices have become increasingly dependent on the use of VLSI circuits. The power of a processor is determined in large part by the multiplier used in its design. Multiplier factor booth coding is being used to reorder the input bits in order to reduce facility use. The booth decoder works by rearranging the specified booth equivalent. The Booth decoder has the ability to expand the range of zeros. As a result, the power consumption of the design will be decreased even more. As soon as the input bit constant drops below zero, related rows or columns of an adder must be disabled, if possible.

Keywords— F_{in} Field-Effect Transistor (F_{in} FET), CMOS (Complementary Metal-Oxide Semiconductor)

I. INTRODUCTION

CMOS has lost its credibility in the area of integrated circuits as a result of the scaling beyond 45 nm method. F_{in} FET-based circuits have been the subject of several studies in the literature. The biggest problem of CMOS transistors is that they use a lot of power and have a lot of leakage current.

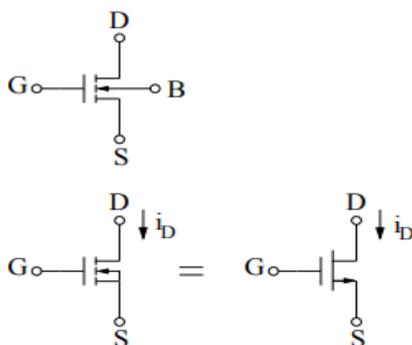


Fig 1.1 Schematic diagram of FET (Filed Effect Transistor)

Many flip flops may share a pulse generator, which reduces power consumption and chip space. Aside from

switching input signals, the speed was practically exactly the same with the addition of an IC Circuit. For example, the clock gated sense amplifier flip flop with variable approach was found to increase design performance, operating speed and produce improved power efficiency. Power supply reduction has been explored in the context of saving energy. By applying an electric field, a field-effect transistor (FET) may change the width of a conducting channel in a semiconductor (hence the term field-effect transistor) JFETs are another form of FET that are not made using the metal-oxide manufacturing process. n-channel and p-channel FETs are available for each of these three groups.

II. LITERATURE SURVEY

Designing VLSI circuits with low power and low voltage is an exciting prospect. In microprocessors and digital signal processors, adding is the most common arithmetic operation. For signed multiplication, the Modified Booth Multiplier is one of the methods to choose from. The quickest multiplier is what it is most often used for. Conventional and GDI (Gate

Diffusion Input) techniques were used to create a low-power 8-bit Modified Booth multiplier.

According to Cadence, a comparative evaluation of all designs was performed using 180nm Technology [2]. An encoder, multiplier, and full adder include the multiplier and Booth encoder with partial product generators, and one-bit adders (half and full). By encoding signed integers to the 2's complement [3], Booth multiplication allows for smaller, quicker multiplication circuits. VLSI architectural design necessitates high-performance, small-footprint, and low-power arithmetic processing units. A multiplier is a crucial component in the design of systems using digital signal processing and other applications. According to research, microprocessor and DSP algorithms conduct multiplication operations in more than 70% of all instructions sent to the processor. Consequently, these processes take longer to complete [4].

VLSI chips are increasingly being used to create more complex signal processing systems[5-8]. The amount of zeros in the multiplicand will grow as a result of this booth decoder. The booth multiplier features a booth decoder that translates the provided input into the booth equivalent. As a result, the design's power consumption may be lowered by reducing the number of switching activities. This component's switching behavior may be predicted by setting the input bit coefficient to zero, which disables all rows and columns [9-12]. The multiplier determines the speed of the CPU.

So there is a need of high speed multiplier. For example, dynamic domino logic gates are quicker and need less space, but total power consumption might be much greater than that of static gates [12-17]. Partially completed products are taken into account when multiplying speed booth multipliers. Speed of partial product increases as booth multiplier reduces necessary partial product by half. An encoder, partial product generating unit, and adder circuit make up the booth multiplier [18-20] converting redundant data to binary. It is possible to get M partial products with N bits in each partial product by multiplying two integers (one with an M-bit multiplicand and one with an N-bit multiplier). In a multiplier, this creates a multiple-forming circuit [21].

III. PROPOSED METHODOLOGY

The different complete adder circuits for low power delay products have been examined. When the adder is run at a lower power or delay, the circuit as a whole performs better and consumes less power. A 10T adder method is a low-power

delay product full adder circuit with a low transistor count. One of a kind 10T delay product complete adder circuits were shown. Tanner EDA tools with 45nm technology are used to simulate the CMOS adder, 10T adder, and the suggested 10T adder's performance in order to assess its viability.

Design and simulation of the full adder and array multiplier were carried out using 45nm Technology and the designs were implemented in the previous standard Gate Diffusion Method (GDI), modified GDI to achieve a good 0and CMOS Technology. The auto-tuned proportional integral derivative controllers are intended for use in situations where load changes are foreseen and where quick and precise control action is required. In order to respond quickly and accurately, Cascade controllers are built. Single-loop controllers may be controlled more effectively with a cascade system controller. Auto-tuning a cascade controller system may be accomplished via a technique known as relay feedback. For a single-loop feedback controller, the standard on-off relay oscillation is prolonged. The cascade controller tuning approach provided in Application is used to achieve the controller's parameter with the lowest possible computational cost. For various supply voltages, sources and delays have been estimated and studied.

The 10T full adder has a considerable delay owing to the circuit's several stages. There is a new 4T XOR gate suggested to solve this issue. There are few transistors in this gate yet it gives great speed and low power consumption at the lowest possible cost. The N_1 , P_2 transistors are turned on and the N_2 , P_1 transistors are turned off when the input combination $a=1$ and $b=0$ is entered. Due to the P_2 transistor, the output is a logic 1 because of input a's logic 1. Similarly Toggling ON the N_2 and P_1 transistors and OFF the N_1 and P_2 transistors is accomplished when $a=0$ and $b=1$.

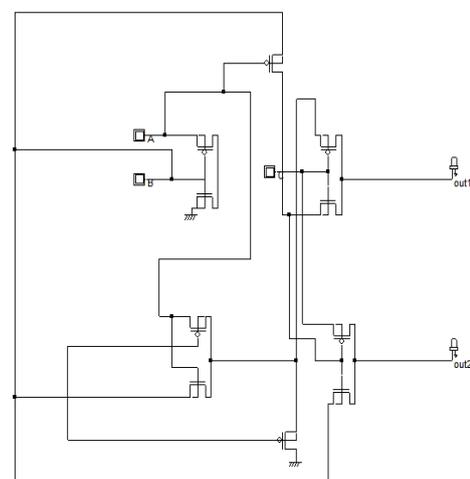


Fig 3.1 Schematic Diagram For The Proposed System

Logic 1 at input b is linked to P₁ transistor, hence the output is logic 1. P₁, P₂ turn on and N₁, N₂ switch off simultaneously when the two inputs are both zero, resulting in a zero-volt output. The original 10-T schematics may be rearranged by substituting safe transmission gates for harmful single-pass transistors that were previously used in the circuit. However, the non-ideal internal levels of the Micro wind XOR gate do not lead to a proper inverter simulation, which has significant detrimental consequences. The simplest way to develop an XOR function is to just implement it.

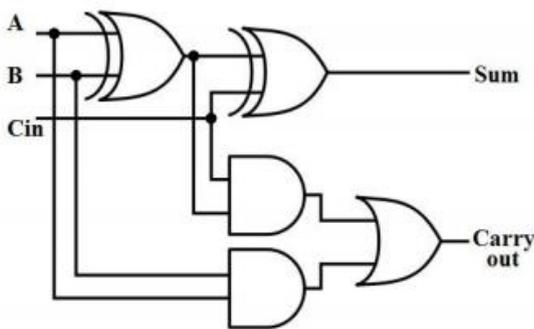


Fig 3.2 Schematic Diagram of full adder using gates

The Full Adder sums the two inputs and returns a value. It may either be used in conjunction with other full adders, or it can be used as a standalone device. This essential building component for circuit applications, full adders have been a major focal area for scientists for several years.

Various logic models, each with its own virtues and limitations, were researched to construct reliable, simpler, with less power consumption, although the on chip space need is generally bigger compared to its dynamic cousin. Different logic approaches may be used to enhance the overall performance of a complete adder in these designs. 2CMOS, CPL, TGA, TFA, Hybrid, 14T, and 16T etc. belong to the first group.

Full adders 10T, 9T, and 8T are part of the second group, which does not have full swing outputs. Since there are less transistors in this kind of XOR-XNOR circuit, the power consumption and heat dissipation are lower, and chip space is also saved.

IV. SIMULATION RESULTS

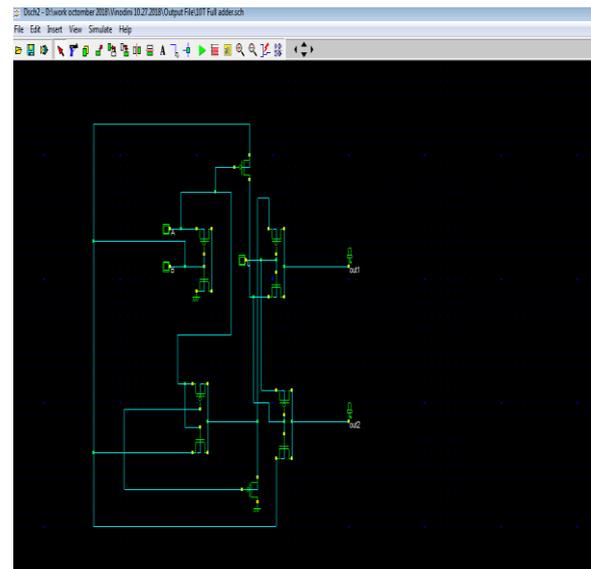


Fig 4.1 Schematic Diagram of 10T Full adder

When $V_{DD}=1v$, the suggested 10T adder delivers power reduction of 41.65 percent compared to Conventional CMOS. In comparison to the 6T adder, the proposed 10T adder saves 41.65 percent electricity and 10.5 percent PDP.

TABLE I. TABULATION FOR 10 T FULL ADDER

Adder type	No of transistor	Power saving	Delay	Input Source
PROPOSED	10	41.65%	360	0.35
EXISTING	6	61.80%	520	2.36

To illustrate the relationship between supply voltage and delay in an 8T adder, we plotted the supply voltages $V_{dd}=1$ volt, $V_{dd}=0.75$ volt, and the proposed 8T adder for each of these values. When can be observed from the graph, as supply voltage V_{DD} is dropped, circuit latency increases.

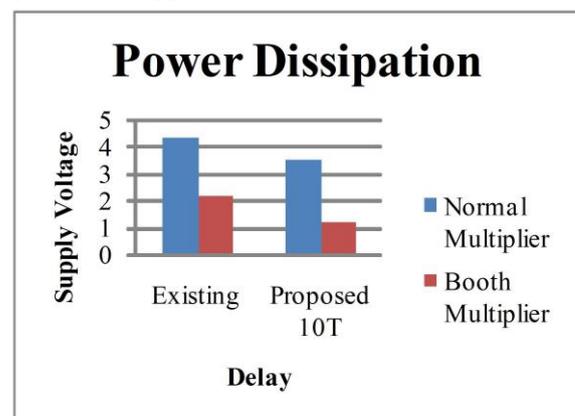


Fig 4.2 Power Dissipation Comparative Chart

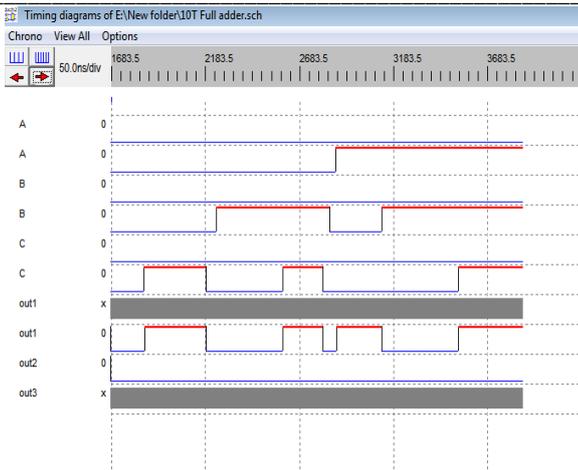


Fig 4.3 Output wave source of 10T Full Adder

A plot of supply voltage and power dissipation for CMOS, 10T and planned 10T adders is shown in Figure 4.3. Voltage V_{DD} can be shown to have an immediate impact on the circuit's average power usage in this figure.

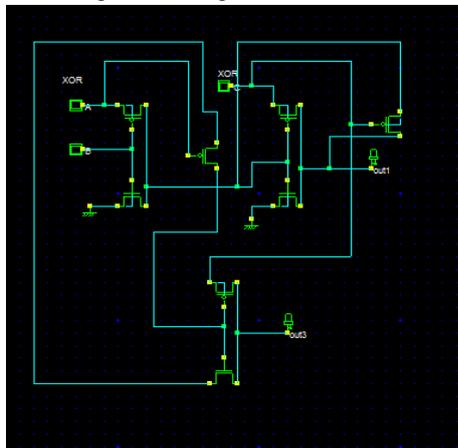


Fig 4.4 Schematic Diagram of 8T Full adder

As $V_{DD}=1v$, the proposed 8T adder saves 29.20% in power when compared to conventional CMOS. The suggested 8T adder additionally delivers power savings of 29.20 percent and PDP savings of 12.3 percent compared to the 4T adder.

TABLE II. TABULATION FOR 8 T FULL ADDER

Adder Type	No of transistor	Power saving	Delay	Input Source
Proposed	8	29.20	230	6.00
Existing	4	49.17	284	0.54

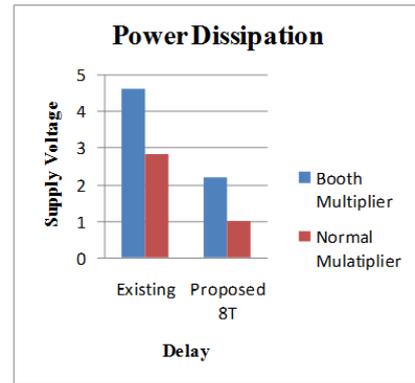


Fig 4.5 Power Dissipation Comparative Chart

With $V_{DD}=1V$ or $V_{DD}=0.75V$ or $V_{DD}=0.75V$ supply voltages, the CMOS adder, a 4T adder and the planned 8T adder all have the same latency. The circuit's propagation delay will grow if the supply voltage V_{DD} is decreased. Increasing the delay reduces the adder's operating speed and efficiency.

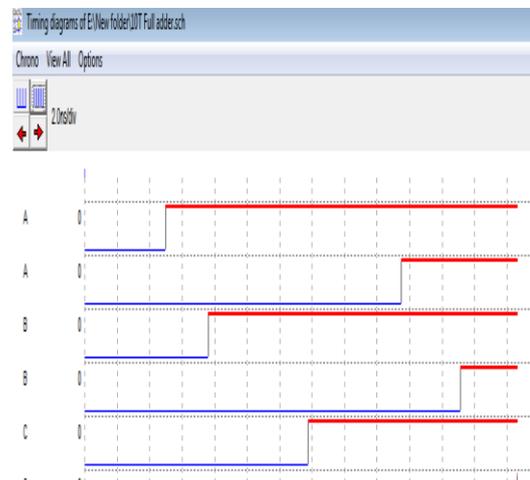


Fig 4.6 Output wave source of 8T Full Adder

Figure 4.6 illustrates supply voltage vs power dissipation for the CMOS adder, 4T adder, and projected 8T adder. Voltage V_{DD} can be shown to have an immediate impact on the circuit's average power usage in this figure.

V. CONCLUSION

XOR gate-based full adder has been shown in this work power and zone productive strategy for transistor-based full adder using suggested transistors. In terms of power consumption, the suggested full adder circuit is compared to previously disclosed full adder circuits. The reduced transistor count in the whole adder exhibits the improved power usage with higher yield flag levels. Operation performed is with high



speed and little leakage. In standby mode, the Power Gating technology decreases the amount of electricity that flows through the system. Different voltage supplies are used to test various parameters.

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