A Review on Control Strategies and Topologies of Multi Level Converter System

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Abstract— In recent decades, high-performance and medium voltage energy management for academia and industry have been attracted by multilevel converter topologies. In addition, the multi-level principle is used without decreasing the inverter power output to synthesise the harmonic distortion on the output waveform. For the reduction of harmonic distortion in the output waveform, the multi-level principle is used. The following topologies are presented: diode clamped inverters (neutral point clamped), condenser clamped (flying condenser), multi-level cascading (dc source, etc.) and the most effective modulation methods built for this converter category: multi-level, selective harmonic removal and space m vectors. A series of different topologies are given in this paper. Multi-level inverters have been gaining popularity in research teams and in the production of industrial applications for high and medium voltage applications for 20 years. Moreover, compared to a conventional converter, multi-level inverters can generate switched waveforms with reduced harmonic slopes. Recently, multi-level inverters have increased interest in their ability to generate high-quality wave forms at lower frequencies; the multi-level topology used in dynamic restaurant voltages reduces the harmonic distortion of the inverter output waveform without inverter output losses. By integrating control techniques for multi-level inverters, this paper discusses the most common topologies, making their implementations flexible in some power applications in many industrial areas.

Keywords- Diode Clamped Inverter, Capacitor Clamped Inverter, Cascade H-Bridge Inverter, Modulation Technique.

I. INTRODUCTION

In Over recent years, multi-level inverters have become popular in the medium and high voltage energy industry. Renewable energy sources, such as fuel cells, solar photovoltaics and wind [1], can interact widely with a multi-level converter system. Waveforms, the fundamental concept for multi-level converters, are synthesised from various voltage levels provided by insulated DC sources or a condenser bank. The description is from the implementation of converter topology by Baker[2]. A significant number of multi-level converter topologies have been proposed over recent decades. Fast modulation schemes and modern converter topologies have also been invented. This literature review has been split into four sections. The first is the literature study, covering the three topologies of multi-level converters: the Neutral Camped Converter, the H-Bridge Cascade and the Flying Converter. The second section explores modulation methods, including vector pulse width and sinusoidal pulse width modulation (SPWM). Finally, the execution of multi-level converters in the industry. Different industries, including renewable energy interface systems and medium-voltage industrial motor drive systems, have started to demand higher-power devices in the last few years[3]. Medium and megawatt electricity levels are required for certain mediumvoltage motor drives and utilities. In high-power and mediumvoltage cases, a multi-story power conversion system was thus introduced as an alternative. Many multi-story topologies for converters were then developed. Just one power semi-conductor switch is not attached to achieve a middle voltage grid. A multifunctional converter also permits the use of renewables, in addition to achieving high amounts of electricity. The term multilevel started with a three-level converter. Compared to conventional two-stage topology, the benefits of 3-stage inverters are. One half of the DC source voltage on the switches is voltage; The switching frequency can be decreased for similar switching losses. With the same switching frequency, the greater output current harmonics are diminished. Various multi-level converter topologies have been proposed over the last two decades. In addition, three similar major multi-level converter structures have been included in the literature: cascaded Hbridges with different dc sources and diode clamping (neutral clamping). In addition, abundant modulation techniques have been developed. Figure.1 shows a diagram of varying degrees of single-phase phase-legged inverters, representing an ideal switch with different positions for power semiconductor operation. A two-level inverter generates an output voltage with two levels in relation to the negative terminal of the condenser, while three-level inverters produce three voltages, the most attractive features are as follows.

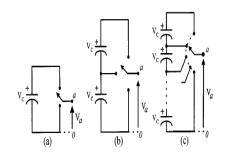


Figure.1: One Phase Leg Of An Inverter With (A) Two Levels, (B) Three Levels, And (C) N Levels.

II. RELATED WORKS

Ethiopia et al. [1] proposed 99.5 percent efficient, all-silicon triphase, seven-level hybrid active neutral clamping point inverter. 1]. [1]. The newest standard for ultra-efficient power intensive converters is discussed in this post: a 3,4 kW/dm3 (55,8 W/in3), a 3-3-3-µm all-Silicon inverter with an efficiency of 99,35 percent. This is why another traditional FCC approach

has been introduced. The gain is that the number of FC units is cut in half by using the DC-link midpoint connection. The valued DC voltage can be easily accessed on the hardware since the condensers have to be connected in number, and the front end of the ANPC level has an appraised switch that is almost the DC bus voltage switch on the front end at the grid frequency.

A six-level photovoltaic asymmetric hybrid inverter with internal MPPT capability was introduced by Caro et al [3]. For medium-voltage networked photovoltaic power stations, the author analyses the asymmetric photovoltaic multi-level hybrid inverter proposed in this article. If the main NPC inverter can effectively and fully monitor the active power flow in the cascade, by using the predicted technique and adjusting the DC input voltage to achieve MPPT. Instead, as an active power philtre, the much smaller auxiliary TL1 controls the phase and amplitude of the output current, but even temporarily. According to the characteristics of the planned technology, different types of power supplies could be almost new to help meet the different requirements of both inverters. The model test performed on the model scale shows that the DC voltage of the NPC inverter input is not balanced, but due to the application of MPPT in the cascade, the PV field is not radiated equally.

Ji. Itoh et.al[4] submitted an experimental multi-level inverter test with an h-bridge clamping circuit for a single-phase tri-wire grid connection. The author addresses a multi-level inverter with an H-bridge clamp circuit in this article, which is intended for 1- β -3-wire network communication. The intended inverter simply needs 12 gate-operated switches to achieve 5 stage output voltage. For a conventional multilevel converter with a grounded DC bus neutral point, 16 switches are compulsory. The grid control plan of the proposed system will be drawn up. In addition, simulation and experimentation on the plan technique of passive modules was deliberate and tested. It is possible to compensate for the unstable voltage of the DC condensing unit using the PI controller.

A comparative study of grid-connected photovoltaic device multilevel inverters was submitted by Jiang and Jiang et al [[5]. In this paper the author analyses 3 primary techniques (NPC, FC and CHB) of 3-a 3-stage inverters suitable for mid-voltage power systems connected to photovoltaic grids. A PV series, a DC-DC converter, a 3-level inverter with a philtre and a grid additive transformer are included in the system. Using MATLAB / Simulink, multi-carrier SPWM controls for entire types of inverters were advanced. The L-C philtre also ensures the waveforms of the voltage and current sinuses. FFT review expressed the final THD results from the recreation of these three-story inverters and were methodically shown in the comparison result plate.

A cascaded Multilevel HERIC inverter was submitted by Kukade et al.[6] to reduce the leakage current in photovoltaic applications. In this paper the author studies a HERIC dependent cascade 9-level MLI to resolve the current problem of leakage in photovoltaic applications. The author of this article discusses the proposed modelling and control strategy for fusion system fusion based on a Permanent Magnet Synchronous Generator (PMSG), which is used for adjustable speed diesel engines and wind turbines in grid- and photovoltaic components. The focus of the planned control strategy is PMSG speed control and DC bus voltage control, active-response power control and PV power operations. The results of the simulation show that the future control methodology is suitable and the controls are precisely identical to the reference variables. Furthermore to change the inverter to provide the power of the linear maximum field, the voltage balance-centered space-vector modulation method is used. It has other advantages, such as the low frequency of switching.

Lawan et al. [8] presented a multi-source power system based on pv battery systems and diesel generators for micro grid applications. Solar hybrid systems are mostly paired with solar diesel generators from photovoltaic systems. The castoff continuously connects the cavity between the present load and the actual power provided by the photovoltaic system. Battery storage is usually included to maximise the solar energy contribution to the overall hybrid system efficiency, due to varying solar energy volumes and partial diesel generation volumes within a given range. This device is intended for those systems which are intended to guarantee the supply of microgrid electricity. By picking an adjustable speed diesel generator, the ingestion of fuel can be optimised. The main areas of the proposed control strategy are PMSG speed control, DC bus tension control and SVPWM active and reactive power control. The results of the simulation indicate that the suggested governor solution is acceptable and that the variables are close to the benchmark. In addition, space vector variant technology based on composite voltage strength, is advantageous for controlling the inverter.

A multi-level inverter with a single-phase H-Bridge Clamp Circuit was discussed by Walnut et al [9], which is suitable for super-junction / SiC MOSFET connectivity. The multi-level inverter with an H-bridge clamping circuit is intended to be used for 1- β 3-wire mains connections. The proposed inverter simply requires 12 controllable switches to achieve a 5-level output voltage. For a conventional multilevel converter with a grounded DC bus neutral point, 16 switches are compulsory. The control system was assessed. In addition, the arithmetic design methodology was also measured and tested by simulation. Finally, compared to the normal ANPC converter, the use of the super interconnection MOSFET would reduce the conduction loss of the clamp circuit by 20.7 percent. The usage of SiC MOSFET would minimise by 42.6 percent the loss of conductivity.

M. Rao et al.[10] discussed the use of conventional two-level inverters for a 4n pole induction drive to provide a multi-level inverter configuration. A multi-level inverter technology for 4th pin motor drives is proposed in this article, optimally derived from inductive motor stator winding systems. A 2-level conservatory inverter switches to the basic frequency in this shape. The lack of switching is thus compact. The thyristor can also be used as a switch for inverters for low-frequency operation, which is also ideal for high-power applications. In the case of conservative NPC or condenser clamp types, the expected topology can be used in any inverter or DC power drop to improve the stability of the system. In the proposed configuration, the need for switching devices is lower than the traditional topology.

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III. CONVERTER TOPOLOGIES

The inverter is an electronic control system that transforms DC power into precise power at the required frequency and output voltage. The converter that produces an output or voltage current with 2 separate voltage levels is a two-level inverter. High switch losses, high frequency switching, and high voltage applications are handled by the simple inverter. Many problems, such as EMI, harmonic distortion and high switch stress, are faced with this kind of reverse engine. In 2-stage inverters, high THD is another problem and it is extremely difficult to directly synchronise semiconductor switches to medium and high voltage grids. Here in current circumstances, we feel the need for various multi-level inverter techniques. In 1975, multilevel inverter technology was introduced with 3-stage inverters. A high power rating is feasible with the help of a high voltage level in the converter. This decreases the transition rate for the converter. From various levels of dc voltage, this type of converter produces a smooth sine waveform.Multi-level inverters have created a stimulating zone in the output requests for high voltage and high power ratings. It can simply be synchronised with renewable energy sources for various high-power applications. The voltage of the DC link, from the rectifier, comes from renewable sources of electricity.

A large number of semi-conductor switches are the main drawback of this system and a separate gate driver circuit has been needed for each switch to increase system difficulty. It is extra costly for the entire system. Researchers are currently working on reducing the number of switches, the system's complexity on the gate driver circuit

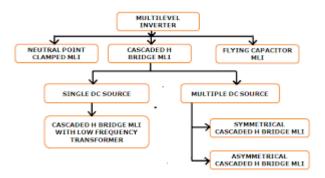


Figure 3 Multilevel Inverter Topologies

This type of Multilevel Converter reveals that it has been known to be the principal type of Multilevel Inverter, the NPC.

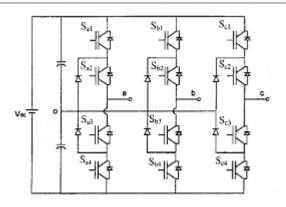


Figure 4 Neutral Point Clamped Multilevel Inverter

As in figure 2, the basic inverter generates an AC output voltage and the DC voltage is used as an input. Using PWM switching techniques, the AC output voltage is produced. The theory of multilevel inverter topology incorporates multiple DC voltage phases consisting of a level output waveform (MLI). In the archived output waveform, a minimum dv / dt and harmonic distortion is present. The circuit system is particularly challenging with the rise in voltage phases. A complex switching system is also required. In this inverter, every leg generates three voltage stages (Vdc /2, 0, -Vdc /2). Except that the clamping diodes are coupled and paired between two condensers, this conversion device is similar to the standard 2-level inverter. The condensers act as DC bus input voltages, each with stimulation of the Vdc/2 voltage. If the number of levels is to be increased, it is possible to increase the relationship to a new phase leg. The zero voltage phase can be created by switching nearer to the middle point. Clamping diodes clamp the transmitted voltage to zero at the neutral stage. As there are more interrupters, clamping diodes and condensers are attached to the output of the converter to produce additional voltage stages. For a multi-level inverter, this results in modern techniques with spaced diodes. The multi-level inverter can be divided into two-thirds of production-based life categories: cascaded H-bridge converter with different dc sources, multi-level diode clamp inverter and flying condenser.Figure 4 demonstrates the 1-µf NPC power circuit. Two conventional two-level inverters were fitted with it. One inverter is fixed above the other for the loading drive. Furthermore, 2 serial-connected diodes between the lower and higher inverters were connected to the neutral mid point N. Condensers here cause the DC bus stress to be removed in two stages. Therefore, consuming an additional source of DC is unacceptable in this case. The transfer is just half of the voltage of the dc link, the transverse voltage. The tension harmonics are based on the double switching frequency. The size of the condenser is restricted and pre-loaded. The converters are used back to back and competence is perfect at fundamental frequency. By expanding any point, clamping diodes are enhanced. The Dc level discharges if control and monitoring is not correct. While practical issues arise for high-performance converters, this system. To reverse the recovery pressure, it requires high-speed clamping diodes. Because of the diode series, the issue with the system is a major concern. This type of multilevel inverter was presented as a Flying Capable (FC), which is calculated as a further development of the multi-level inverter system. The custom of condensers is based on this inverter. It is made through the connection of a number of

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switching devices with condenser clamping. Unfinished stress is passed to electrical equipment by condensers. In FC, the substitute officer is the same as the NPC. However, clamping diodes do not need this topology of multi-level inverters. These converters benefit from balancing FC in the dismissal process. It has the capability to track the movement of reactive and active power. The main downside of the half-bridge of the FC inverter is that its voltages are almost below the DC voltage input. It avoids issues with the clamping diode. It reduces the device strain from dv / dt. Assistance in preserving the charge balance in condensers with additional switching conditions. It has smaller switching capabilities. This type of multilevel inverter has defined the fundamental evidence of transformer technology, with its capacity for multilevel product voltages through the source of many DCs.[11]

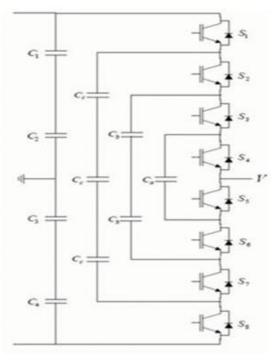


Figure 5 Flying Capacitor Multilevel Inverter

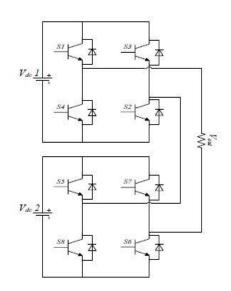


Figure 6 Cascaded H-bridge (CHB) Multilevel Inverter

A series of 1-3 inverters is associated and modelled with this technique. Eight semiconductor switches and 5 inverter levels are fitted with the H-bridge circuit. The DC input is attached to the H-bridge and provides 5 output levels of voltage. These outputs vary from -2Vdc to +2Vdc for the control of 4 switches. This H-bridge sequence is connected to the output and synchronisation of multilevel inverters. The voltage steps in an H-bridge inverter are computed by n=2s+1. S- The number of DC sources and n- the inverter's output stage. The multilevel inverter in Figure 6 shows the Cascaded H-bridge (CHB). A mew type of converter is an active clamped inverter (ANPC) that overwhelms the insufficient piece of raw losses between external and internal switches that have finished positioning power switches instead of normal diodes[10].

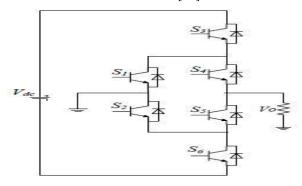


Figure 7 Active NPC Multilevel Inverter

Figure 4.8 below shows the ANPC multilevel converter, which blends NPC and FC inverter techniques. This preparation achieves the 2-stage inverter (n-1)/2 quantity when n is the output stage of the inverter. In each section of the technique, there are 4 inverters that are used to achieve a nine-phase inverter.

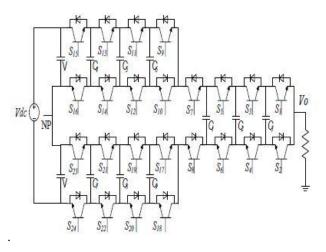


Figure 8 Active NPC Multilevel Inverter

Therefore, for each portion of this technique, 4 2-stage inverters were cascaded here to be supplied with an inverter of nine stages. There are three main sections in this form of multi-level ANPC converter. The main section contains the 9 switches to 16 and the 4, 5 and 6 condensers, but the 7 to 24 switches and the 7, 8 and 9 condensers are included in the supplementary portion of the inverter. One switches to eight and one, two, three condensers are used in three sections of this inverter and the inverter is connected to the load.

IV. CONTROL STRATERGIES

It is easy to hit F Staircase waveform, but to correct this a larger philtre could create more output distortion. Therefore in order to achieve better voltage rates for DC current sources based on a chopper, a sinusoidal PWM method is suggested.Small inductors which simultaneously decide the amplitude of the wave form of the PWM output are used to present the design of the five-story inverter. With the proposed multi-level topology, this reduces the inductor power, gateway circuit complexity and complete harmonic distortion of output current[15].

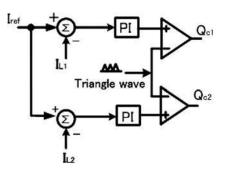


Figure 9. Controller diagram of chopper circuits

The pulse-width modulation Field Programmable Gate Array (FPGA) provides flexible sinusoidal output with enhanced efficiency for single-phase five-tier inverters. Compared to other works mentioned in this paper, the multi-level inverter output can be modified on the programme stage and provides greater flexibility and a new approach. FPGA In terms of control technique, this is created digitally by the Altera DE2 Board's multi-carrier PWM. PWM signals are produced via a sinewed reference signal and two triangular carrier signals through the pulse generator block at the same frequency. Simulations, including Sine LUT, Modulation Index, Carrier LUTs, Comparators and Pulses Logic[17], are carried out from the diagram given for the pulse generator block. The dynamic voltage restore (DVR) supports the load voltage in the case of a voltage deflection, and the voltage swell compensation can be supplied with the expansion voltage compensation (Figure 2). North Carolina was the first DVR to be constructed in 1996. The use of a multilevel cascaded inverter for DVR control with two discontinuous SVM techniques reduces switching losses. The system of SVM decreases your losses. The most precious PWM technology is SVM for ML converters that enhance the use of DC bus and cause lower losses of commutation. The modulation index can be defined as an inverter at the M level. During sampling period, discontinuous SVM is used to clamp down the first step while the remaining two are switched. In an experimental study carried out on 11-kV 5-MVR DVR cascaded multilevel inverters, this PWM technique enables DVR to maintain the same harmonic output using traditional multi-level SVM technique[18].

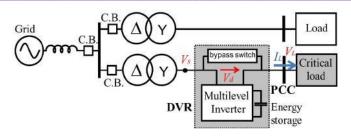


Figure 10. DVR in a distribution system

DVR in a method of delivery Two carrier-based modulation techniques for a two-level inverter topology allow high quality, multi-level wavelengths and power sharing. It described the following modulation techniques based on the carrier: Continuous modulation (symmetrical placement of zero vectors).Discontinuous modulation of modulation (during the switching time it does not have zero vectors). The drawbacks of both techniques are removed with both techniques used in one PWM algorithm, and the dual two-level inverter is properly modulated[19]. A spectral analysis for multi-level modulation using the double technique of the Fourier series becomes impractical when it comes to processes with standard samples and multi-level vector offsets. Nevertheless, the solution is possible using the spectral image with the single-dimensional functions of the one-dimensional Fourier series, with separate PWM waveforms and expansion lateral band base.

V. CONCLUSION

The paper presented an overview of the multilevel inverter topologies for several scientific literatures and their modulation technique. In order to produce more and more consumer goods, the multilevel inverter structure is now being used, and multilevel inverter technologies are being researched and developed worldwide. This paper does not cover or refer to all the work in this partnership, but it has systematically applied the basic principle of different inverters. In order to locate important sources, this survey report, as well as previous work on inverter topologies and their modulation technology, will be very useful for researchers. Several multi-level inverter topologies and control methods have been modified to allow engineers to employ acceptable technologies to use multi-level converters for more grid-integrated renewable energy systems. Removing the transformers of the energy system achieves substantial volume and weight efficiency, reduces the size of the system and loss of power. Wind turbine inverters, photovoltaic centralised converters, pumped hydro storage, etc. are currently available in a range of commercial products. This trend is likely to remain stable, and with more grid codes, increased system power consumption, increased semiconductor power generation and multi-level technology advantages, more implementations will be introduced. Multi-level converters can be effectively used as a power distribution system based on a variety of energy sources and networks of varying voltage levels to achieve a distributed generation system.

REFERENCES

[1] Anderson, John Augustus. "Power-conditioned solar charger for directly coupling to portable electronic devices." U.S. Patent No. 9,088,169. 21 Jul. 2015.

- [2] Guo, Qijie, et al. "Fabrication of 7.2% efficient CZTSSe solar cells using CZTS nanocrystals." Journal of the American Chemical Society 132.49 (2010): 17384-17386.
- [3] Testa, A., et al. "A buck-boost based dc/ac converter for residential PV applications." International Symposium on Power Electronics Power Electronics, Electrical Drives, Automation and Motion. IEEE, 2012.
- [4] Le, Hoai Nam, and Jun-Ichi Itoh. "Inductanceindependent nonlinearity compensation for singlephase grid-tied inverter operating in both continuous and discontinuous current mode." IEEE Transactions on Power Electronics 34.5 (2018): 4904-4919.
- [5] Dahal, R., J. Li, K. Aryal, J. Y. Lin, and H. X. Jiang. "InGaN/GaN multiple quantum well concentrator solar cells." Applied Physics Letters 97, no. 7 (2010): 073115.
- [6] Kukde, Harsha, and A. S. Lilhare. "Solar powered brushless DC motor drive for water pumping system." 2017 International Conference on Power and Embedded Drive Control (ICPEDC). IEEE, 2017.
- [7] Nie, Wanyi, Hsinhan Tsai, Reza Asadpour, Jean-Christophe Blancon, Amanda J. Neukirch, Gautam Gupta, Jared J. Crochet et al. "High-efficiency solutionprocessed perovskite solar cells with millimeter-scale grains." Science 347, no. 6221 (2015): 522-525.
- [8] Sahoo, Saroja Kanti, and Nudurupati Krishna Kishore. "Battery state-of-charge-based control and frequency regulation in the MMG system using fuzzy logic." IET Generation, Transmission & Distribution (2020).
- [9] Ichikawa, Yukimi, Yoshiaki Osawa, Hiroshi Noge, and Makoto Konagai. "Theoretical studies of silicon heterojunction solar cells with rib structure." AIP Advances 9, no. 6 (2019): 065117.
- [10] Haripriya, T., Alivelu M. Parimi, and U. M. Rao. "Performance evaluation of DC grid connected solar PV system for hybrid control of DC-DC boost converter." In 2016 10th International Conference on Intelligent Systems and Control (ISCO), pp. 1-6. IEEE, 2016.
- [11] Saha, Swarup Kumar. "Optimization Technique Based Fuzzy Logic Controller for MPPT of Solar PV System." 2018 International Conference on Emerging Trends and Innovations In Engineering And Technological Research (ICETIETR). IEEE, 2018.
- [12] Patel, Hiren, and Vivek Agarwal. "MATLAB-based modeling to study the effects of partial shading on PV array characteristics." IEEE transactions on energy conversion 23.1 (2008): 302-310.
- [13] Satapathy, Susree Sukanya, and Nishant Kumar. "Modulated Perturb and Observe Maximum Power Point Tracking Algorithm for Solar PV Energy Conversion System." 2019 3rd International Conference on Recent Developments in Control, Automation & Power Engineering (RDCAPE). IEEE, 2019.
- [14] Wang, Hui, and Yun Hang Hu. "Graphene as a counter electrode material for dye-sensitized solar cells." Energy & Environmental Science 5.8 (2012): 8182-8188.
- [15] Tahiri, F. E., K. Chikh, M. Khafallah, A. Saad, and D. Breuil. "Modeling and performance analysis of a solar PV power system under irradiation and load

variations." In 2017 14th International Multi-Conference on Systems, Signals & Devices (SSD), pp. 234-238. IEEE, 2017.

- [16] Kumar, Nallapaneni Manoj, Ramjee Prasad Gupta, Mobi Mathew, Arunkumar Jayakumar, and Neeraj Kumar Singh. "Performance, energy loss, and degradation prediction of roof-integrated crystalline solar PV system installed in Northern India." Case Studies in Thermal Engineering 13 (2019): 100409.
- [17] Sharma, Rahul S., and P. K. Katti. "Perturb & observation MPPT algorithm for solar photovoltaic system." In 2017 International Conference on Circuit, Power and Computing Technologies (ICCPCT), pp. 1-6. IEEE, 2017.
- [18 Zakaria, N. Z., H. Zainuddin, S. Shaari, S. I. Sulaiman, and R. Ismail. "Critical factors affecting retrofitted roof-mounted photovoltaic arrays: Malaysian case study." In 2013 IEEE Conference on Clean Energy and Technology (CEAT), pp. 384-388. IEEE, 2013.
- [19] Ghosh, Swapnendu Narayan. "Improvised Binary Sequence MPPT Method for Solar PV Applications." In 2018 2nd IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), pp. 234-238. IEEE, 2018.
- [20] Fossum, J.G., 2017. Physical operation of back-surfacefield silicon solar cells. IEEE Transactions on Electron Devices, 24(4), pp.322-325..